IN THE DRAWINGS

Formal drawings (Figs. 1A-1E) are filed herewith.

REMARKS

This responds to the Office Action dated January 30, 2006. Claims 8 and 31 are amended; as a result, claims 1-34 are now pending in this application.

Title

The title has been amended to make it more clearly indicative of the invention to which the claims are directed, as required by the Examiner.

Drawings

Formal drawings of Figs. 1A-1E are submitted herewith, as required.

§112 Rejection of the Claims

1. Claims 5-6, 16-17 and 25-26 were rejected under 35 U.S.C. § 112, first paragraph, as lacking adequate description or enablement. Applicant respectfully traverses the rejection.

The Office Action states that the claims "all state that a sequence of values are formed by concatenating a portion of each respective addressing value of the first vector of addressing values to a respective one of a sequence of numbers ... yet there is no disclosure of what the sequence of numbers can or has to be, or what their intended purpose is."[1]

The purpose is to identify the elements in a vector register having the same addresses. Typically a vector is loaded with addresses of operands and the operands are fetched according to the addresses to perform an operation. If elements in a first vector have the same address the first result will be correct, but results downstream will be incorrect because the downstream results will be based on an old operand. This is explained on page 4 line 4 through page 5 line 23 of the present application. To identify the addresses that occur multiple times, a second vector is formed having data elements of a sequence of numbers appended or concatenated to part of the addresses in the first vector. This is shown in FIG. 1A. This second vector is then written to a scratch area of memory in element order according to a part of the of the addresses in the first vector. If there are multiple occurrence of an address, the address will be written multiple times and will finally contain the last element of the second vector to be written to that

[1] Office Action, pg. 3.

address. FIG. 1A also shows that elements read-back from the scratch area of memory will be different from the those written where the addresses are used multiple times. Thus, comparing the read-back element values to the written element values will identify the identical addresses through mis-compares.

The present application states that since the identities of the elements in the vector register 112 having the same addresses are unknown, the present invention provides a way to determine these elements.[2] The present application also teaches that data values of the first sequence of values are each formed by concatenating a portion of each respective addressing value of the first vector of addressing values to a respective one of a consecutive sequence of integer numbers.[3] FIG. 1A shows an example where the data values are formed by concatenating the sequence consecutive integers 0 to E-1 to the addressing values in vector register 112. The present application further teaches that the values are written in element order.[4] A second sequence of values is read back from the sequence of addressed locations values resulting from the storing of the first sequence to obtain a second sequence of values. An example is given in the present application.[5] FIG. 1A includes an example of the second sequence 116 and indicates the miscompares where vector register 112 had the same addresses. Applicant respectfully submits that the specification of the present application adequately enables and describes the subject matter of the claims at issue and requests reconsideration and allowance of claims 5-6, 16-17 and 25-26.

2. Claim 8 was rejected under 35 U.S.C. § 112, first paragraph, as lacking adequate description or enablement. Claim 8 is amended to better recite the claimed subject matter. No new matter is entered.

§103 Rejection of the Claims

3. Claims 1-10 and 20-29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard et al. (US 5,640,524, "Beard") in view of Bruckert et al. (US 5,068,851, "Bruckert"),

[2] Patent Application, pg. 7 lines 3-5.
[3] Patent Application, pg. 12 lines 11-13.
[4] Patent Application, pg. 7 lines 14-17.
[5] Patent Application, pg. 7 lines 5-26, FIG. 1A.

and further in view of Ernst et al., "Cyclone: A Broadcast-Free Dynamic Instruction Scheduler with Selective Replay" (ISCA-2003, "Ernst").

Applicant respectfully traverses the rejection. One criterion to establish a *prima facie* case of obviousness is that the prior art reference (or references when combined) must teach or suggest all the claim limitations.[6] Additionally, a claim in dependent form shall be construed to incorporate by reference all of the limitations of the claim to which it refers.[7]

Regarding claims 1-10:

Applicant cannot find in the proposed combination of Beard, Bruckert and Ernst any disclosure of, among other things,

> storing a first sequence of values to a sequence of addressed locations within a constrained area of memory, reading back from the sequence of addressed locations values resulting from the storing of the first sequence to obtain a second sequence of values, and performing an arithmetic-logical operation using values from the third vector register and the compressed second vector of operand values to generate a result vector

as recited in claims 1 and 10 and incorporated into claims 2-9.

The Office Action states that the elements are taught in Beard.[8] However, the cited portions of Beard refer to main memory storage locations of the data words,[9] whereas the present patent application associates the constrained area of memory with a scratch area of memory.[10] Also, Applicant cannot find any disclosure of obtaining a second sequence of values by reading back from the sequence of addressed locations values resulting from the storing of the first sequence, as recited in claims 1 and 10. The cited portions of Beard refer to retrieving data words from main memory, storing the data words in a second vector register, and performing an operation upon the retrieved data words and storing the results in a third vector register or storing the results in main memory,[11] and do not include disclosure of obtaining such a second sequence. Further, Applicant is unable to find in the cited portions of Beard any disclosure of a compressed second vector.

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[6] M.P.E.P. § 2143.
[7] 35 U.S.C. § 112 ¶4.
[8] Office Action, pg. 5.
[9] Beard, col. 3 lines 1-5 and lines 14-22.
[10] Patent Application, pg. 5 line 12 and FIG. 1A
[11] Beard, col. 3 lines 1-22.

Additionally, Applicant cannot find in the proposed combination of Beard, Bruckert and Ernst any disclosure of,

> comparing the first sequence of values to the second sequence of values to generate a bit vector representing compares and miscompares,

as recited in claims 1 and 10. The Office Action asserts that Beard fails to teach the element, [12] but that "Bruckert teaches comparing two values, one from a primary source, and one from a secondary source to verify if the data is in agreement.[13] However, Bruckert states that "only a single thirty-two bit data bus 85 is provided between the CPU module 30 and memory module 60," and "therefore, memory module 60 cannot compare two sets of data from memory controllers 70 and 75."[14] In Bruckert, "data integrity is verified by ... checking the two separate sets of ECC signals that are transmitted."[15] Thus, Bruckert does not teach or suggest comparing a first sequence of values to a second sequence of values to generate a bit vector.

Further, Applicant cannot find in the proposed combination of Beard, Bruckert and Ernst any disclosure of,

> compressing the second vector of operand values using the bit vector, and using the first vector of addressing values as masked by the bit vector, loading a third vector register with elements from memory,

as recited in claims 1 and 10.

The Office Action states that Beard fails to teach the elements,[16] but that "Ernst teaches compressing the second vector by marking certain instructions as invalid (Section 2.4, by marking the instruction invalid, it is compressing in the sense that the vector contains less useful information), and using those values, loading a third vector register with elements from memory (Section 2.4, the invalid instructions must replay, which when combined with Beard's invention, would require those particular instructions to be read out into another vector correctly)."[17]

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[12] Office Action, pg. 5.
[13] Office Action, pg. 6 citing Bruckert, col. 13 lines 9-57.
[14] Bruckert, col. 13 lines 28-32.
[15] Id., lines 32-35.
[16] Office Action, pg. 5.
[17] Office Action, pg. 6.

However, the cited portions of Ernst refer to speculation masks used to identify mispeculated instructions.[18] Thus, even if the Applicant were to acquiesce to the statement in the Office Action concerning the teachings of Ernst, the combination of Beard, Bruckert and Ernst would still contain no teaching or suggestion of using addressing values as masked by the bit vector that is generated from comparing the sequence values to load a third vector register. Also, Ernst refers to where,

> "The speculation mask of each instruction is included with the instruction in the Cyclone scheduler queues. When instructions reach the end of the main queue, they probe the speculation state. If the table indicates that the instruction has been squashed it is dropped."[19]

Thus, Ernst apparently uses a speculation mask to retire rather than load an instruction.

Concerning claim 5, Applicant cannot find in the proposed combination of Beard, Bruckert and Ernst any disclosure of,

> wherein data values of the first sequence of values are each formed by concatenating a portion of each respective addressing value of the first vector of addressing values to a respective one of a sequence of numbers,

as recited in the claim. The Office Action states that the subject matter is taught in Beard because it is common practice as is shown in the Computer Architecture Lecture pgs. 11 and 12.[20] However, the Computer Architecture Lecture is concerned with sign extending to fit a value from a memory location of a smaller size to a memory location of a larger size and does not address the subject matter of claim 5.

Claim 5 read with claim 1 includes, among other things,

> storing a first sequence of values to a sequence of addressed locations, wherein data values of the first sequence of values are each formed by concatenating a portion of each respective addressing value of the first vector of addressing values to a respective one of a sequence of numbers.

An example of a sequence of values is shown in FIG. 1A in vector Vseq0. The elements are formed by concatenating a sequence (in this example 0, 1, 2, 3, ... E-1) onto a portion of the address (represented by @'0, @'1, ...@'(E-1)). Thus, the proposed combination of Beard,

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[18] Ernst, section 2.4.
[19] Id.
[20] Office Action, pg. 8.

Bruckert and Ernst with the Computer Architecture Lecture does not teach or suggest the elements recited or incorporated into claim 5.

A second criterion required to establish *prima facie* obviousness, is that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.[21] The teaching or suggestion to make the claimed invention and the reasonable expectation of success must be found in the prior art, and not in applicant's disclosure.[22]

Beard refers to a vector processing system,[23] and that vector read ports 116 are coupled to the V register input multiplexor 295 via pipeline holding elements 299 and error checking and correcting circuits 301.[24] Bruckert refers to a method and apparatus for testing the operation of modules for use in a fault tolerant computing system that consists of two distinct computing zones[25] and states that "only a single thirty-two bit data bus 85 is provided between the CPU module 30 and memory module 60," and "therefore, memory module 60 cannot compare two sets of data from memory controllers 70 and 75."[26] Applicant submits that proper motivation is lacking to combine Beard with Bruckert because Beard already refers to a system with error checking and combining Beard with the ECC signal checking of Bruckert would apparently result in an inferior error checking system.

Concerning the proposed addition of Ernst to the combination, the M.P.E.P. states that there are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art.[27] In regards to the nature of the problem to be solved, the Office Action states that one of ordinary skill in the art would recognize the advantage in selectively reloading/replaying in that only a few instructions must be re-executed.[28] However, the present application states that since the identities of the elements in the vector register 112 having the same addresses are unknown,

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[21] M.P.E.P. § 2143.
[22] M.P.E.P. § 2143, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).
[23] Beard, Abstract.
[24] Beard, col. 12 lines 31-33.
[25] Bruckert, Abstract.
[26] Bruckert, col. 13 lines 28-32.
[27] M.P.E.P. § 2143.01, citing *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).
[28] Office Action, pg. 6.

the present invention provides a way to determine these elements.[29] Thus, a combination of Beard and Ernst would be directed toward the problem of recovery from mis-speculation of instructions and not toward identifying elements in a vector having the same addresses.

In regards to the teachings of the references, Applicant is unable to find a motivation to combine Beard and Ernst in the references themselves. In regards to the knowledge of persons of ordinary skill in the art: although the Office Action states that one of ordinary skill in the art would recognize the advantage in selectively reloading/replaying in that only a few instructions must be re-executed, Ernst states that later instructions that access this invalid register will replay and indicate that their result is unavailable, forcing a cascaded dependence-based instruction replay.[30] Thus, one of ordinary skill in the art would recognize that many instructions rather than a few may have to be replayed. Applicant respectfully submits that the Office Action fails to establish *prima facie* obviousness because proper motivation to combine Beard, Bruckert and Ernst has not been shown.

Regarding claim 20:

Claim 20 depends on base claim 11 and incorporates all of the elements of that claim. Applicant believes that claim 20 is allowable at least for the reason as discussed below that the proposed combination of Beard and Bruckert does not teach or suggest all the elements of claim 11. The addition of Ernst fails to teach or suggest the missing elements. For example, Applicant cannot find in the proposed combination of Beard, Bruckert, and Ernst any disclosure of

> using the first vector of addressing values as masked by the bit vector, loading a third vector register with elements from memory; and performing an arithmetic-logical operation using values from the third vector register and the compressed second vector of operand values to generate a result vector,

as recited in claim 11 and incorporated into claim 20.

Additionally, Applicant cannot find in Beard, Bruckert, or Ernst

> wherein data values of the first sequence of values are each formed by combining at least a portion of each respective addressing value of the first vector register of addressing values to a respective one of a consecutive sequence of integer numbers,

[29] Patent Application, pg. 7 lines 3-5.
[30] Ernst, section 2.4.

as recited in claim 20. The Office Action states that the subject matter is taught in Beard because it is common practice as is shown in the Computer Architecture Lecture pgs. 11 and 12.[31] However, the Computer Architecture Lecture is concerned with sign extending to fit a value from a memory location of a smaller size to a memory location of a larger size. An example of a sequence of integer numbers concatenated onto an address is shown in FIG. 1A in vector Vseq0. The elements are formed by concatenating a sequence (here, 0, 1, 2, 3, ... E-1) onto a portion of the address (represented by @'0, @'1, ...@'(E-1)). Thus, the Computer Architecture Lecture does not describe the subject matter recited in claim 20.

Regarding claims 21-29:

Applicant cannot find in the proposed combination of Beard, Bruckert and Ernst any disclosure of, among other things,

> circuitry that selectively loads the third vector register with elements from memory addresses generated from the first vector register of addressing values as masked by the bit vector register, and circuitry that selectively performs an arithmetic-logical operation on corresponding values from the third vector register and the compressed second vector of operand values to generate values of a result vector,

as recited in claim 21 and incorporated into claims 22-29. The Office Action states that the elements are taught in Beard.[32] However, the cited portions of Beard refer to a method and apparatus that stores in a first vector register offset address values, retrieves data words from main memory and stores the data words in a second vector register, and performing an operation upon the retrieved data words and storing the results in a third vector register or storing the results in main memory.[33]

> Also, Applicant cannot find in Beard, Bruckert and Ernst any disclosure of
>
> circuitry that selectively stores a first sequence of values to a sequence of addressed locations within a constrained area of memory,

as recited in claim 21. The cited portions of Beard refer to main memory storage locations of the data words,[34] whereas the present patent application associates the constrained area of memory

[31] Office Action, pg. 8.
[32] Office Action, pg. 14.
[33] Beard, col. 2 line 67 - col. 3 line 22.
[34] Beard, col. 3 lines 1-5 and lines 14-22.

with a scratch area of memory.[35] Additionally, Applicant cannot find in Beard, Bruckert, or Ernst any disclosure of

> circuitry that selectively loads, from the sequence of addressed locations, values resulting from the stores of the first sequence to obtain a second sequence of values,

as recited in claim 21. The cited portions of Beard refer to retrieving data words from main memory, storing the data words in a second vector register, and performing an operation upon the retrieved data words and storing the results in a third vector register or storing the results in main memory,[36] and do not include disclosure of circuitry that obtains such a second sequence.

Additionally, Applicant cannot find in the proposed combination of Beard, Bruckert and Ernst any disclosure of,

> circuitry that selectively compares the first sequence of values to the second sequence of values to generate bit values into the bit vector register representing compares and miscompares,

as recited in claim 21. The Office Action states that "Bruckert teaches comparing two values, one from a primary source, and one from a secondary source to verify if the data is in agreement.[37] However, Bruckert states that "only a single thirty-two bit data bus 85 is provided between the CPU module 30 and memory module 60," and "therefore, memory module 60 cannot compare two sets of data from memory controllers 70 and 75."[38] In Bruckert, "data integrity is verified by ... checking the two separate sets of ECC signals that are transmitted."[39] Thus, Bruckert does not teach or suggest comparing a first sequence of values to a second sequence of values to generate a bit vector.

Further, Applicant cannot find in the proposed combination of Beard, Bruckert and Ernst any disclosure of,

> circuitry that selectively compresses the second vector of operand values using the values in the bit vector register, and circuitry that selectively loads the third vector register with elements from memory addresses generated from the first vector register of addressing values as masked by the bit vector register,

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[35] Patent Application, pg. 5 line 12 and FIG. 1A
[36] Beard, col. 3 lines 1-22.
[37] Office Action, pg. 15 citing Bruckert, col. 13 lines 9-57.
[38] Bruckert, col. 13 lines 28-32.
[39] Id., lines 32-35.

as recited in claim 21.

The Office Action states that "Ernst teaches compressing the second vector by marking certain instructions as invalid (Section 2.4, by marking the instruction invalid, it is compressing in the sense that the vector contains less useful information), and using those values, loading a third vector register with elements from memory (Section 2.4, the invalid instructions must replay, which when combined with Beard's invention, would require those particular instructions to be read out into another vector correctly)."[40]

However, Ernst refers to where "[m]ispeculated instructions are identified using speculation masks.[41] Thus, even if the Applicant were to acquiesce to the statement in the Office Action concerning the teachings of Ernst, the combination of Beard, Bruckert and Ernst would still contain no teaching or suggestion of circuitry that uses addressing values as masked by the bit vector that is generated from comparing the sequence values.

Also, Applicant cannot find in Ernst circuitry that loads a third vector register with elements from memory using the first vector of addressing values as masked by the bit vector. Ernst refers to where,

> "The speculation mask of each instruction is included with the instruction in the Cyclone scheduler queues. When instructions reach the end of the main queue, they probe the speculation state. If the table indicates that the instruction has been squashed it is dropped."[42]

Thus, Ernst apparently uses a speculation mask to retire rather than load an instruction.

In sum, the Office Action fails to make a proper *prima facie* case of obviousness because the proposed combination of Beard, Bruckert and Ernst fails to teach or suggest all the limitations of the claims and because proper motivation is lacking to combine Beard, Bruckert and Ernst. Applicant respectfully requests reconsideration and allowance of claims 1-10 and 20-29.

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[40] Office Action, pg. 15.
[41] Ernst, section 2.4.
[42] Id.

4. Claims 11-20 and 30-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard et al. (US 5,640,524) in view of Bruckert et al. (US 5,068,851). Applicant respectfully traverses.

Regarding claims 11-20:

Applicant cannot find in the proposed combination of Beard and Bruckert any disclosure of, among other things,

> using the first vector of addressing values as masked by the bit vector, loading a third vector register with elements from memory; and performing an arithmetic-logical operation using values from the third vector register and the compressed second vector of operand values to generate a result vector,

as recited in claim 11 and incorporated into claims 19-20.

The Office Action states that the elements are taught in Beard.[43] However, the cited portions of Beard refer to a method and apparatus that stores offset address values in a first vector register, retrieves data words from main memory and stores the data words in a second vector register, and performing an operation upon the retrieved data words and storing the results in a third vector register or storing the results in main memory.[44]

Also, Applicant cannot find in Beard or Bruckert any disclosure of

> storing a first sequence of values to a sequence of addressed locations within a constrained area of memory,

as recited in claim 11. The cited portions of Beard refer to main memory storage locations of the data words,[45] whereas the present patent application associates the constrained area of memory with a scratch area of memory.[46] Additionally, Applicant cannot find in Beard or Bruckert any disclosure of

> reading back from the sequence of addressed locations, values resulting from the stores of the first sequence to obtain a second sequence of values,

as recited in claim 11. The cited portions of Beard refer to retrieving data words from main memory, storing the data words in a second vector register, and performing an operation upon

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[43] Office Action, pg. 22.
[44] Beard, col. 2 line 67 - col. 3 line 22.
[45] Beard, col. 3 lines 1-5 and lines 14-22.
[46] Patent Application, pg. 5 line 12 and FIG. 1A

the retrieved data words and storing the results in a third vector register or storing the results in main memory,[47] and do not include disclosure of circuitry that obtains such a second sequence.

Additionally, Applicant cannot find in the proposed combination of Beard and Bruckert any disclosure of,

> comparing the first sequence of values to the second sequence of values to generate bit values into the bit vector register representing compares and miscompares,

as recited in claim 11. The Office Action states that "Bruckert teaches comparing two values, one from a primary source, and one from a secondary source to verify if the data is in agreement.[48] However, Bruckert states that "only a single thirty-two bit data bus 85 is provided between the CPU module 30 and memory module 60," and "therefore, memory module 60 cannot compare two sets of data from memory controllers 70 and 75."[49] In Bruckert, "data integrity is verified by ... checking the two separate sets of ECC signals that are transmitted."[50] Thus, Bruckert does not teach or suggest comparing a first sequence of values to a second sequence of values to generate a bit vector.

Regarding claim 30:

Applicant cannot find in the proposed combination of Beard and Bruckert any disclosure of, among other things,

> means for storing a first sequence of values to a sequence of addressed locations within a constrained area of memory, wherein each one of these location's addresses in the constrained area of memory is based at least in part on a subset of a corresponding one of the addressing values,

as recited in claim 30. The cited portions of Beard refer to main memory storage locations of the data words,[51] whereas the present patent application associates the constrained area of memory with a scratch area of memory.[52] Additionally, Applicant cannot find in Beard or Bruckert any disclosure of

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[47] Beard, col. 3 lines 1-22.
[48] Office Action, pg. 15 citing Bruckert, col. 13 lines 9-57.
[49] Bruckert, col. 13 lines 28-32.
[50] Id., lines 32-35.
[51] Beard, col. 3 lines 1-5 and lines 14-22.
[52] Patent Application, pg. 5 line 12 and FIG. 1A

> means for loading from the sequence of addressed locations values resulting from the storing of the first sequence to obtain a second sequence of values,

as recited in claim 30. The cited portions of Beard refer to retrieving data words from main memory, storing the data words in a second vector register, and performing an operation upon the retrieved data words and storing the results in a third vector register or storing the results in main memory,[53] and do not include disclosure of structure that obtains such a second sequence.

Additionally, Applicant cannot find in the proposed combination of Beard, Bruckert and Ernst any disclosure of,

> means for comparing the first sequence of values to the second sequence of values,

as recited in claim 30. The Office Action states that "Bruckert teaches comparing two values, one from a primary source, and one from a secondary source to verify if the data is in agreement.[54] However, Bruckert states that "only a single thirty-two bit data bus 85 is provided between the CPU module 30 and memory module 60," and "therefore, memory module 60 cannot compare two sets of data from memory controllers 70 and 75."[55] In Bruckert, "data integrity is verified by ... checking the two separate sets of ECC signals that are transmitted."[56] Thus, Bruckert does not teach or suggest structure for comparing a first sequence of values to a second sequence of values.

Regarding claims 31-34:

Applicant cannot find in the proposed combination of Beard and Bruckert any disclosure of, among other things,

> a circuit that determines elements of the first vector register that have an address value that duplicates an address value in another element,

as presently recited in claim 31 and incorporated into claims 32-34. The Office Action states that beard fails to teach the element,[57] and that Bruckert teaches comparing two values, one from

[53] Beard, col. 3 lines 1-22.
[54] Office Action, pg. 15 citing Bruckert, col. 13 lines 9-57.
[55] Bruckert, col. 13 lines 28-32.
[56] Id., lines 32-35.
[57] Office Action, pg 29.

a primary source, and one from a secondary source to verify if the data is in agreement.[58] However, Bruckert states that "memory module 60 cannot compare two sets of data from memory controllers 70 and 75."[59] In Bruckert, "data integrity is verified by ... checking the two separate sets of ECC signals that are transmitted."[60] Thus, Bruckert also does not teach or suggest the element.

In sum, the Office Action fails to establish a proper *prima facie* case of obviousness because the proposed combination of Beard and Bruckert do not teach or suggest all of the elements of claims 11-20 and 30-34, and because, as discussed above, proper motivation is lacking to combine Beard and Bruckert. Applicant respectfully requests reconsideration and allowance of claims 11-20 and 30-34.

[58] Id., citing co. 13 lines 9-57 of Bruckert.
[59] Bruckert, col. 13 lines 28-32.
[60] Id., lines 32-35.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 1st day of May, 2006.

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